IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Czech et al	**GROUP:**	2826
SERIAL NO:	09/852,123	**EXAMINER:**	Johannes P. Mondt
FILED:	May 8, 2001		
FOR:	ELECTROSTATIC DISCHARGE PROTECTIVE STRUCTURE		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REPLY BRIEF

This Reply Brief is in response to the Examiner's Answer dated September 13, 2006. This Reply Brief is being submitted in response to the new grounds of rejection set forth in the Examiner's Answer.

Entry of this reply brief is respectfully requested.

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date below, with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

/Patrick O'Shea/
Patrick J. O'Shea

11/13/2006
Date

REJECTION UNDER 35 U.S.C. §102 – AVERY

CLAIM 1

The Examiner's Answer cites a new grounds of rejection that claim 1 is anticipated by the subject matter disclosed in Avery. This rejection was not presented in the Official Action from which the present appeal was taken, and thus was not discussed in the Appellant's brief. We shall now discuss why the rejection of claim 1 for allegedly being anticipated by Avery is improper.

This new rejection takes a position with respect to the teaching of Avery in shocking conflict with the position previously taken by the office. This conflict can plainly be summarized as the Examiner's position in the last Official Action from which this appeal is taken is to night, as the new position set forth in the Examiner's Answer is to day. Specifically, the Official Action dated February 13, 2002 stated *"Avery does not necessarily teach a single-track resistor to precede every control connection in order to enable a large input surge voltage to be more uniformly dispersed."*. (Official Action dated February 13, 2002, pg. 4). Similarly, the Official Actions dated November 15, 2002; June 19, 2003 and April 20, 2004 all make the same contention that Avery does not necessarily teach a single-track resistor to precede every control connection in order to enable a large input surge voltage to be more uniformly dispersed. Thus during the course of four Official Actions, during which the feature in claim 1 in question remain unchanged, the Examiner consistently took a position with respect to what Avery teaches that is in shocking conflict with contrary position set forth in the Examiner's Answer.

Clarifications to arguments are to be expected during an appeals process, but 180 degree shifts with respect to how the USPTO interprets a prior art reference is not, and as such are properly barred under the legal doctrine of *Law of the Case*. That is, when the USPTO consistently applies an

interpretation to a prior art reference over the over course of numerous Official Actions, the USPTO's interpretation of the prior art reference must also continue into subsequent prosecution stages, such as the present appeal, absent some extraordinary circumstances by the USPTO regarding why such an 11th hour change in the way the prior art reference is construed is proper. Specifically, up until the Examiner's Answer the USPTO took a position with respect to the teachings of Avery that is opposite to its current position. Hence, it is respectfully submitted that the legal doctrine of *Law of the Case* applies in this matter, preventing the USPTO from now applying a new contrary interpretation to the alleged teachings of Avery.

Even if the new construction of Avery were to be applied, a fair and proper reading indicates that Avery is still incapable of anticipating the subject matter of claim 1. The Examiner's Answer relies upon FIG. 7. However, Avery makes it clear that the circuit illustrated in FIG. 7 is merely *"...the effective equivalent circuit of the protection device of FIGS. 1-5...."* (emphasis added, col. 6, lines 37-38). As known in art, an equivalent circuit is simply a mathematic mechanism for representing an electrical network. An equivalent circuit is not the actual structure of the circuit. In contrast, FIG. 1 of Avery is described as a schematic plan top view of the layout of the structure of the invention (see col. 3, lines 27-28). As shown in FIG. 1, the gate electrode 34 runs to only the shorter length channel structure 16, and not to the longer channel length structures 18a-18d. As known a 35 U.S.C. §102(b) rejection requires that a single prior art reference disclose each feature of the claimed invention. It is respectfully submitted that Avery is incapable of anticipating claim 1 since Avery fails to disclose at the least the claimed feature of *"a single track resistor (RB) co-integrated into a semiconductor body, wherein said single track resistor precedes every control connection (B) of said laterally designed bipolar transistors (T1-T3)."* (cl. 1).

REJECTION UNDER 35 U.S.C. §103 – AVERY IN VIEW OF SMITH

CLAIMS 2-5

It is respectfully submitted that this rejection is now moot, since claim 1 is patentable for at least the reasons set forth above. We shall now discuss the combination of Avery and Smith.

Claim 2 recites:

> "wherein said semiconductor body has embedded therein at least one emitter zone and at least one collector zone of the first conduction type and at least one base zone of the second, opposite conduction type, wherein a well-shaped region is inserted into said semiconductor body between said zones of the first conduction type and said base zone or said base zones, so as to extend the effective mean free path of the charge carriers to said base zone." (emphasis added, cl. 2)

It is recognized that Avery does not teach such a well shaped region (see the Examiner's Answer, pg. 4). It is then alleged that Smith discloses such a well and that a skilled person would have modified the subject matter disclosed in Avery to include such a well.

A fair and proper reading reveals that Smith has nothing to do with ESD protective devices. Smith simply discloses a stacked gate buffer. Although FIG. 1 of Smith illustrates a block labeled ESD circuit 15**, Smith clearly states that this ESD circuit 15 is not disclosed within the specification or figures of the patent (see Smith, col. 3, lines 51-56).** Specifically, Smith states *"[t]he ESD circuit 15 may be any standard ESD circuit that is well known in the art. The structural detail of the ESD circuit 15 is not necessary for one of ordinary skill in the art to make or use the stacked-gate buffer 30 of the present invention and, accordingly, such detail will not be provided herein."* (Col. 3, lines 51-56). Merely mentioning an ESD circuit in patent does not make ESD protective devices the subject matter of the patent. The reference as a whole must be considered.

In addition, the deeper doped region 80 referred to in Smith has nothing to do with an ESD device. For example, **FIG. 1 shows that the deeper doped region 80 is associated with the**

stacked buffer and not the ESD structure. Hence, it is respectfully submitted that a skilled person working in the field of ESD devices would not combine Smith with Avery since Smith does not relate to ESD devices.

REJECTION UNDER 35 U.S.C. §103 – AVERY IN VIEW OF SMITH AND LI

CLAIM 6

Claim 6 currently stands rejected under 35 U.S.C. §103 for allegedly being obvious in view of the combined subject matter disclosed in Avery, Smith and U.S. Patent 5,623,387 to Li et al (hereinafter "Li").

It is respectfully submitted that this rejection is now moot, since claim 1 is patentable for at least the reasons set forth above, along with claims 2-5.

REJECTION UNDER 35 U.S.C. §103 – AVERY IN VIEW OF SMITH AND WONG

CLAIMS 7-10 AND 12

Claims 7-12 currently stand rejected under 35 U.S.C. §103 for allegedly being obvious in view of the combined subject matter disclosed in Avery, Smith, Li and U.S. Patent 6,277,689 to Wong et al (hereinafter "Wong").

It is respectfully submitted that this rejection is now moot, since claim 1, claims 2-5 and claim 6 are patentable for at least the reasons set forth above.

CONCLUSION

For all the foregoing reasons, we submit that the rejection of claims 1-12 is erroneous and reversal thereof is respectfully requested.

If there are any additional fees due in connection with the filing of this appeal brief, please charge them to our Deposit Account 50-3381. If a fee is required for any extension of time under 37 C.F.R. §1.136 not accounted for above, such an extension is requested and the fee should be charged to the above Deposit Account.

Respectfully submitted,

Patrick J. O'Shea
Reg. No. 35,305
O'Shea, Getz & Kosakowski, P.C.
1500 Main Street, Suite 912
Springfield, MA 01115
(413) 731-3100, Ext. 102